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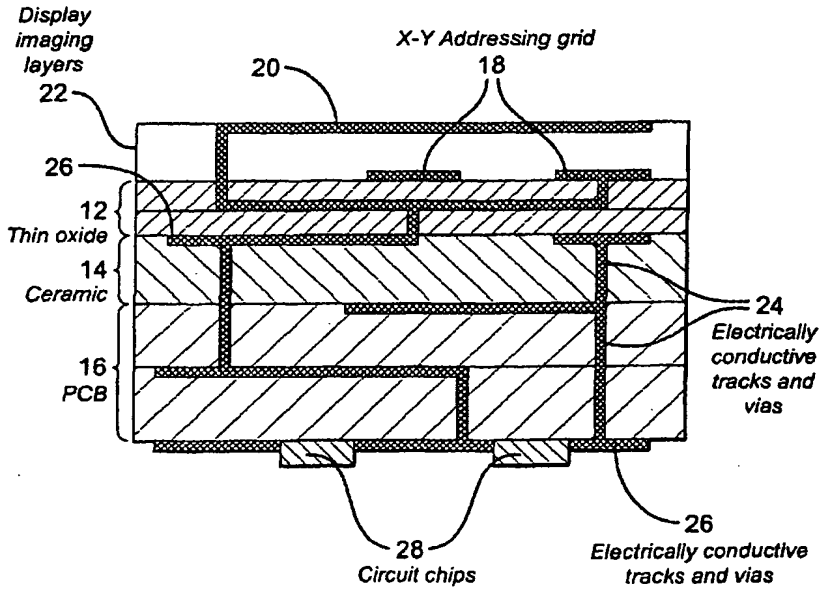
(54) Title: ELECTRONIC DEVICE



(57) Abstract: A display device (10) consists of a plurality of sacked interconnecting systems. Each system is a generally planar substrate having a plurality of connections (24) extending from an upper surface of the substrate to an cpposing lower surface and with the arrangement of connections within each layer being different. Further connecting tracks (26) are provided between adjacent substrate to provide links between the connections (24) in adjacent substrates.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

ELECTRONIC DEVICE

Field of the invention

This invention relates to electronic devices comprising a plurality of circuit elements located on a substrate and in particular, but not exclusively, to devices comprising an array of the same or similar elements located on and/or above a substrate, such as for example matrix addressable devices.

Examples of matrix addressable devices include active or passive matrix flat panel display devices, imaging devices, microsystem arrays, micromechanical systems, and the like.

In this specification, the terms "upper" and "lower" refer to a device when arranged with the array of circuit elements in a generally horizontal plane and facing upwards. The term "circuit element" refers to elements with a passive or active function, such as electrodes, light emitting or light sensing-elements, optoelectronic. elements, micromechanical elements, radio frequency elements, various kinds of transducers, or any combination thereof. The term "electronic device" is used in a broad sense as meaning any device which operates on electronic principles and is intended to embrace devices such as optoelectronic devices, electromechanical devices, radiation sensitive devices, and the like.

Background of the Invention

Conventionally, devices such as flat panel displays are produced on glass or silicon substrates. This is because these materials are very convenient to use, the surfaces are very smooth and rigid and active elements like transistors can be defined directly under pixels. Contact pads are defined near the edge of the substrate (see Figure 1 of the accompanying drawings). The device is then connected to the drive electronics using the contact pads. One of the drawbacks of this arrangement is that a significant fraction of the surface area of the substrate is not utilised by the active elements. Therefore the effective display area is reduced by that fraction. Another drawback is that the drive electronics for devices such as a matrix addressable device is accommodated on a separate substrate with interconnecting wires between the drive electronics and the substrate containing the active elements.

There is an increasing demand for devices with higher packaging density, maximum space utilisation, higher reliability, higher switching speed and mechanical stability. Accordingly, it is an aim of this invention to provide devices, associated methods and equipment which provide improvements in at least some of these fields.

Summary of the Invention

According to one aspect of the invention, there is provided an electronic device comprising:

- an upper generally planar substrate means carrying a plurality of upper circuit elements and including a plurality of connecting means connected to the circuit elements and passing to the lower surface of the upper substrate means, and
- a lower generally planar substrate means provided adjacent the lower surface of the upper substrate means and including a plurality of connecting means electrically connected to the connecting means of the upper substrate means and passing to the lower surface of the lower substrate means,

wherein the first and second substrate means comprise different interconnect systems.

Examples of interconnect systems include:

- Silicon wafer systems,
- Glass systems,
- Ceramic systems,
- Thin oxide systems (MTO),
- Polymer systems, and
- Printed circuit board systems (PCB).

As technology advances, further systems may develop and so we refer herein to such systems collectively as "interconnect systems."

It should be noted that a silicon wafer is not conventionally regarded as an interconnect system, but in the present invention it may serve as such, by supporting connecting means such as interconnect tracks and vias. All of the systems with the

exception of silicon wafer may be either a single or multilayer system; silicon wafer is always a single layer system.

An interconnect system is characterised by being generally made up of one or more layers of the same material.

Preferred embodiment of the invention overcomes at least some of the drawbacks noted with existing devices by using a combination of materials and techniques where a first interconnect system defines a substrate on which the circuit elements are defined and includes a plurality of connecting means which pass the signal to the lower side of the interconnect system. Instead of the device having contact pads around the edge which connect to a separate board containing the associated processing electronics, in the preferred embodiments the connecting means are used to connect to a second (lower) interconnect system which is attached directly by means of bonding (e.g. chemical, electrochemical etc) or physical attachment to the first interconnect system to provide a hybrid arrangement.

Thus the preferred embodiments allow a composite or modular arrangement where the interconnects are routed in an overall downward direction from the circuit elements on the upper surface of the first substrate means down to the drive or processing electronics circuits which are electrically connected and may be physically attached to the lower surface of the lower most interconnect system. Using this concept, almost the entire surface area of the substrate defined by the uppermost interconnect system can be reserved for defining active elements.

Preferably, each of the upper and lower interconnect systems comprises a single or a multiple layer structure of layers of material.

In addition, the device may include one or more further interconnect systems stacked below the lower interconnect sytem with the further interconnect systems including respective connecting means for co-operation with the connector means in the other interconnect system to pass electrical signals from the circuit elements to the underlying substrate means, in an overall direction substantially out of the plane of the device.

Preferably, the lower or lowermost interconnect system includes means for connection to one or more active circuit means for processing signals from or passing signals to, the circuit elements on the upper interconnect system. For example, the lower or lowermost interconnect system may have attached thereto one or more electronic circuits for processing signals passed to or from the circuit elements on the upper interconnect system.

The connecting means may comprise interconnecting tracks extending generally within the plane of the associated interconnect system, with via means extending from one side of an interconnect system (or a constituent layer) to the other.

In one arrangement the upper circuit elements make up an addressable matrix device.

The addressable matrix device may take many forms but in one arrangement the upper circuit elements may comprise detector pixels. In another arrangement, the upper circuit elements may comprise display pixels.

The use of the hybrid technology of this invention allows the different interconnect systems to complement each other with each being selected according to the particular function it is to perform. Thus for example, in one embodiment, a display is provided on a multi-layer ceramic substrate with the drive circuit mounted at the back of the ceramic. In this particular embodiment, a hybrid arrangement is provided which comprises an upper interconnect system defining a substrate of, for example, multi-layer thin oxide (MTO) on which are fabricated active light producing elements. The lower interconnect system in this embodiment could for example be a single layer ceramic system including conductive tracks and interconnect vias. The single layer ceramic system may be provided with driver electronics circuits on the underside thereof. Both the upper and lower interconnect systems would include interconnected connection means which pass signals from the driver electronics to the display pixels. This particular arrangement has several advantages. The device may employ high conductivity interconnect metals such as copper, aluminium or gold which may be used in conjunction with the multi -layer thin oxide, instead of

molybdenum or titanium or tungsten which typically are used for multi-layer co-fired ceramics. In a conventional arrangement using multi-layer ceramic such as aluminium oxide, the co-firing temperature is typically in the region of 1200°C and this excludes the use of copper, aluminium or gold as interconnect metals, due to their low melting temperature. Certain displays require special ceramics such as that referred to as "zero shrink" to ensure that the interconnect tracks and vias are not dislocated during co-firing. The hybrid arrangement of the preferred embodiment described above would not require this because a multi-layer ceramic is not used. . Accordingly, this may provide a significant reduction in the manufacturing cost of the display.

Furthermore the vias defined in a multi-layer thin oxide system can have a significantly reduced diameter (5 to 10 microns) as compared to multi-layer ceramic substrate where the via diameter is typically of the order of 50 to 100 microns. This is because, in multi-layer structures, the minimum diameter achievable is usually of the same order as the thickness of the layer. In multi-layer ceramic materials, the minimum layer thickness is of the order of at least 50 microns and typically 100 microns. However, in multi-layer thin oxide systems it is possible to achieve several layers of interconnects in a few microns thickness. Leading to an increased packing density for conductors. In addition, the much reduced conductor track widths achievable in this manner allow an increase in the definition of the display because a track width of typically up to 10 microns in multi-layer thin oxides is achievable compared to the 100 microns typical track width in multiple layer ceramic materials. Accordingly the pixel size in a device in which the tracks are laid down in the multi-layer thin oxide can be significantly reduced, giving a higher definition display. The use of a multi-layer thin oxide as the upper substrate means that standard optical lithography and semiconductor processing techniques can be used to define pixellated structures on the substrate.

Furthermore, a field emission display comprising a ceramic substrate and a glass faceplate requires a high vacuum seal between the glass (faceplate) and the ceramic substrate, which we achieve in accordance with our International Application No. PCT/US98/20816. An FED requires the shape and location of the microtips to be

extremely precisely defined. In one hybrid arrangement in accordance with the present invention, the microtips are defined on a MTO or glass surface rather than on a ceramic surface. This may be easier to achieve because of the greater surface smoothness and reduced surface defects of oxide or glass surfaces compared to ceramics.

In general, it is difficult to produce ceramic substrates which are "defect-free", Various types of defects are created when ceramic powders are mixed and sintered. The resulting surface can cause the production high-quality devices directly on the surface to be awkward, where active elements are sensitive to surface quality such as field emission cathodes in FE displays. In such a situation, one embodiment of the invention would use the ceramic layer only as a single layer interconnect for connecting the drive electronics at the back and to act as a support. The front face of the ceramic may be coated with an MTO interconnect system (consisting of tracks and vias) using standard semiconductor processing. In another embodiment a single or a multilayer class interconnect system consisting of tracks and vias may be attached to a single layer ceramic plate, with the drive electronics at the back. The active elements (i.e. the field emission cathodes) can be defined on the glass surface or the MTO which has a much better surface than a ceramic.

Depending on the circuit requirements, the driver electronics for the circuit elements can be mounted directly on the back of the ceramic interconnect system or a further interconnect system (for example a PCB) may be stacked beneath the ceramic and the electronics may be mounted at the back of the PCB.

In another embodiment, to provide an electroluminescent (EL) display such as light emitting polymers (LEPs) a multi-layer polymer (e.g. multi-layer polyimide) or a multi-layer thin oxide may be used in a hybrid arrangement with a ceramic or glass interconnect system. Thus a substrate formed by an interconnect system made of one or more polymide layers supporting a high density of conducting tracks can be used on top of a single or multi-layer ceramic interconnect system, giving a high density of signal lines running through a material of very low dielectric constant. In this way, the delay in the propagation of signals can be reduced considerably.

With the exception of high vacuum sealing, which is not required for EL displays, all the advantages identified for field emission displays apply for both light emitting polymer displays and electroluminescent displays in general.

In other embodiments, a multi-layer polymer interconnect system may be used directly on a multi-layer PCE. Electroluminescent displays require very low power to operate and therefore the heat generated is small compared to other types of displays. As a result the polyimide is unlikely to degrade significantly during operation.

The hybrid arrangement of the invention may also be used for other devices such as, liquid crystal displays is (LCDs), plasma display panels (PDPs) and vacuum fluorescent displays (VFDs) etc, and any combination thereof, resulting in highly compact and high definition displays.

Furthermore, the hybrid architecture may also be used for imaging devices such as charge coupled devices (CCDs) which have a plurality of pixellated arrays of sensing elements which will benefit very significantly from the hybrid arrangement. Again the architecture will mean that these devices will be more compact, with faster response times and less expensive to produce.

Still further, the hybrid arrangement may be used for any light emitting or light sensing devices, optoelectronic devices, micromechanical devices, RF devices, various kinds of transducers etc. or any combination thereof which can be fabricated on a glass, silicon or ceramic substrate where a significant number of connections are required to be made to active elements, including light producing, light sensing, radiation detection, and the like.

In another aspect, this invention provides a method of producing an electronic device consisting in the steps of:-

- providing an upper generally planar substrate means,
- forming a plurality of circuit elements thereon,
- providing a plurality of connecting means passing between the circuit elements and the lower surface of the upper substrate means,

- providing a lower generally planar substrate means, and
- providing a plurality of connection means electrically connected to the connecting means of the upper substrate means and passing to the lower surface of the substrate means,

wherein the first and second substrate means comprise different interconnect systems.

The invention also extends to electronic equipment incorporating an electronic device as described above.

Whilst the invention has been described above, it extends to any inventive combination of the features set out above or in the following description.

In our earlier International patent application, No. PCT/US98/20813, published on 8th April 1999 under No. WO 99/17330 ("Our Earlier International Application"), we described and claimed:

a field effect emission device for a visual display comprising:

- a substrate and
- an emission layer on one face of the substrate, the emission layer having:
  - a multiplicity of emitters and gates, arranged as an array of emission pixels and
  - conductive connections in the emission layer to the emitters and the gates;
- the substrate having:
  - conductive vias provided through the substrate or at least a front layer thereof to at least some of the the conductive connections in the emission layer for electrical connection to their emitters and gates.

In this specification, we refer to the type of field emission device described in Our Earlier International Application as our Front-Layer-Via FED Device.

Our Front-Layer-Via FED Device can be combined with a printed circuit board in accordance with the invention.

Accordingly in accordance with a preferred feature of the invention, there is provided a visual display comprising:

- a field effect emission device for a visual display having:
  - a substrate and
  - an emission layer on one face of the substrate, the emission layer having:
    - a multiplicity of emitters and gates, arranged as an array of emission pixels and
    - conductive connections in the emission layer to the emitters and the gates,
  - the substrate having:
    - conductive vias provided through the substrate or at least a front layer thereof to at least some of the said conductive connections in the emission layer for electrical connection to their emitters and gates;
- an anode sealed to the substrate; and
- a printed circuit board to which the substrate is abutted and directly electrically connected.

Normally the substrate will be a ceramic material multilayer.

It is possible for the printed circuit board to be directly connected to a front face of the substrate, at one or more regions peripheral to the anode. However, it is preferred for the printed circuit board to be connected to the back face of the substrate. This can be via a solder ball grid array (BGA).

Preferably, the substrate has one or more driver circuit chips attached to its back surface, also by another solder ball grid array. This solder has a higher temperature melting point than that of the substrate/printed circuit board BGA. Where the number of connections and/or the physical integrity of the arrangement requires it, the printed circuit board can have a contoured edge or a cut-out for accommodating the driver chip(s) within the plane of the printed circuit board.

Normally, the printed circuit board will have a microprocessor and a keypad mounted thereon, the display being controlled by the microprocessor.

The Drawings

To help understanding of the invention, a specific embodiment thereof will now be described by way of example and with reference to the accompanying drawings, in which:

Figure 1 is a schematic view of a prior art flat panel display device;

Figure 2 is a cross-sectional view through a hybrid interconnect system in accordance with this invention;

Figure 3 is an exploded view of a passive matrix electroluminescent device in accordance with this invention;

Figure 4 is a exploded view, similar to Figure 3, but showing an active matrix electroluminescent device;

Figure 5 is a scrap cross-sectional side view of main components of a visual display of the invention;

Figure 6 is an underneath view of the visual display of Figure 5; and

Figure 7 is a perspective view of the display on a printed circuit board.

Referring initially to Figure 2, there is shown a display or an imagine device 10 in accordance with this invention. In this example, the device comprises three stacked interconnect systems, namely a two-layer thin oxide (MTO) interconnect system 12, a single layer ceramic interconnect system 14 and a two-layer PCB interconnect system 16. The upper MTO interconnect system has formed thereon and in conjunction with the above layer an array of circuit elements, here in the form of column electrodes 18 which form in conjunction with row electrodes 20 an X-Y addressing grid. On top of the upper substrate formed by the upper interconnect system is a display/imaging layer 22.

Each of the systems 12, 14 and 16 comprises an interconnect system made up of filled vias 24 and conductive tracks 26 to provide the required interconnect topology between the active circuit elements 18 on the upper surface of the upper substrate 12 and a number of driver chips 28 provided on the lower surface of the lower-system 16.

Referring now to Figure 1, there is shown schematically a passive electroluminescent display 30. The display built up on a hybrid interconnect structure comprising a multi-layer thin oxide substrate 32 as the upper layer and a ceramic or glass single layer system 34. Each of these systems is provided with interconnects and filled vias in a similar manner as shown in Figure 2, to provide the required interconnects between a driver chip 36 attached to the lower surface of the lower substrate 34 and the column electrodes 40 of which only two are shown. From the column electrodes 40 upwards, the structure is fairly conventional. Accordingly the structure comprises a transparent face plate 42 (e.g. of glass), transparent row electrodes 44 (e.g. of indium tin oxide (ITO)) a first insulator layer 46, a phosphor layer 48, and a second insulator layer 50.

Referring now to Figure 4, the active matrix electroluminescent device is again built up on a hybrid structure, here comprising an upper substrate 52 of silicon wafer, silicon on insulator (SOI) or polysilicon and a lower system 54 of ceramic or glass. As previously, a driver chip 56 is shown attached to the lower surface of the lower system 54 and the required interconnect topology between the driver chips 56 and a number of switch transistors 58 is provided by vias and tracks 60, 62 respectively. Stacked above this, from the top layer down, are a transparent sealing plate 64 transparent electrodes 66, a first insulator layer, a phosphor layer 70, a further insulator layer 72.

The design and manufacture of suitable interconnect systems as described above is well within the competence of one skilled in the art, suitable guidance being obtainable from publications such as "Microelectronic Materials. ", CRM Grovenor, IOP Publishing Ltd 1989, and "Handbook of Polymer Coatings for Electronics", J.J. Licari, L.A. Hughes, Noyes Publications 1990, the entire contents of which are incorporated herein by reference.

The embodiments described above each comprises a hybrid arrangement of two or more interconnect systems, where an interconnect system is defined as a single or multi-layer arrangement of conductive tracks or vias in a particular material. Several distinct interconnect systems have been described above. In all devices the circuit elements are generally defined on the upper surface of the top system and the

driver electronics is electrically connected and may be physically attached to the back of the lower system.

Referring now to Figures 5, 6 & 7, there shown are a number of the main components of a mobile telephone, in particular a main printed circuit board (PCB) 101, a set of keys 102 for a key pad connected on a top surface of the PCB, a main processor 103 connected to the under surface of the PCB, a display 104.

The display is an FED display, having a ceramic multi-layer substrate 105 for providing interconnection between an emission layer 106 and a driver circuit 107. An anode 108 is connected to the substrate via a carrier 109. The driver circuit is electrically connected by a higher temperature solder ball grid array 110, with epoxy infill 111.

The PCB and the substrate are electrically connected, for power supply and video data to be fed to the driver circuit, by another ball grid array 112 of lower temperature solder and equally of with an epoxy infill 113. Although the solder 111 is of lower temperature melting point than that of the BGA 110, to allow its flowing without disturbing the BGA 110, it is equally of higher temperature than that for flowing solder for the main processor and other components (not shown) on the PCB.

It should be noted that to accommodate the driver circuit 107, the PCB has a cut-out 114. The display/PCB BGA 112 is provided peripherally of the driver circuit 107 and around an edge region of the PCB at the cut-out 114.

The man skilled in the art will of course appreciate that a variety of other circuit components are required in the PCB to complete the mobile telephone.

CLAIMS:

1. An electronic device comprising:
   - an upper generally planar substrate means carrying a plurality of upper circuit elements and including a plurality of connecting means connected to the circuit elements and passing to the lower surface of the upper substrate means, and
   - a lower generally planar substrate means provided adjacent the lower surface of the upper substrate means and including a plurality of connecting means electrically connected to the connecting means of the upper substrate means and passing to the lower surface of the lower substrate means,

wherein the first and second substrate means comprise different interconnect systems.

2. An electronic device according to Claim 1, wherein the or each of the upper and lower substrate means comprises a multiple layer structure of layers of material.

3. An electronic device according to Claim 1 or Claim 2 which includes one or more further substrate means stacked below the lower substrate means, the further substrate means including respective connecting means for co-operation with the connecting means in the other substrate means to pass electronic signals from the circuit elements to the underlying substrate means, in an overall direction substantially out of the plane of the device.

4. An electronic device according to any one of the preceding Claims, wherein the lower or lowermost substrate means includes means for connection to one or more active circuit means for processing signals from or passing signals to the circuit elements on the upper substrate means.

5. An electronic device according to any one of the preceding Claims, wherein the connecting means comprise one or more of interconnecting track portions extending generally within the plane of the associated substrate means, and via means extending in a direction generally through the plane of the associates substrate means.

6. An electronic device according to any one of the preceding Claims, wherein the upper circuit elements make up an addressable matrix device.

7. An electronic device according to any one of the preceding Claims, wherein the upper circuit elements comprise detector pixels.

8. An electronic device according, to any one of the preceding Claims, wherein the upper circuit elements. comprise display pixels.

9. A visual display comprising:
   - a field effect emission device for a visual display having:
     - a substrate and
       - an emission layer on one face of the substrate, the emission layer having:
         - a multiplicity of emitters and gates, arranged as an array of emission pixels and
         - conductive connections in the emission layer to the emitters and the gates,
     - the substrate having:
       - conductive vias provided through the substrate or at least a front layer thereof to at least some of the said conductive connections in the emission layer for electrical connection to their emitters and gates;
   - an anode sealed to the substrate; and
   - a printed circuit board to which the substrate is abutted and directly electrically connected.

10. A visual display as claimed in claim 9, wherein the substrate is a ceramic material multilayer.

11. A visual display as claimed in claim 9 or claim 10, wherein the printed circuit board is directly connected to a front face of the substrate, at one or more regions peripheral to the anode.

12. A visual display as claimed in claim 9 or claim 10, wherein the printed circuit board is connected to the back face of the substrate.

13. A visual display as claimed in claim 11 or claim 12, wherein the connection of the printed circuit to the substrate is via a solder ball grid array (BGA).

14. A visual display as claimed in any one of claims 9 to 13, wherein the substrate has one or more driver circuit chips attached to its back surface.

15. A visual display as claimed in claim 13, wherein:
   - the connection of the printed circuit to the substrate is via a solder ball grid array (BGA), and
   - the substrate has driver circuit chips attached to its back surface by another solder ball grid array, having a higher temperature melting point than that of the substrate/printed circuit board BGA.

16. A visual display as claimed in claim 14 or claim 15, wherein the printed circuit board has a contoured edge or a cut-out for accommodating the driver chip(s) within the plane of the printed circuit board.

17. A visual display as claimed in any one of claims 9 to 16, wherein the printed circuit board has a microprocessor and a keypad mounted thereon, the display being controlled by the microprocessor.

18. A method of producing an electronic device consisting in the steps of:-

- providing an upper generally planar substrate means,
- forming a plurality of circuit elements thereon,
- providing a plurality of connecting means passing between the circuit elements and the lower surface of the upper substrate means,
- providing a lower generally planar substrate means, and
- providing a plurality of connection means electrically connected to the connecting means of the upper substrate means and passing to the lower surface of the substrate means,

wherein the first and second substrate means comprise different interconnect systems.

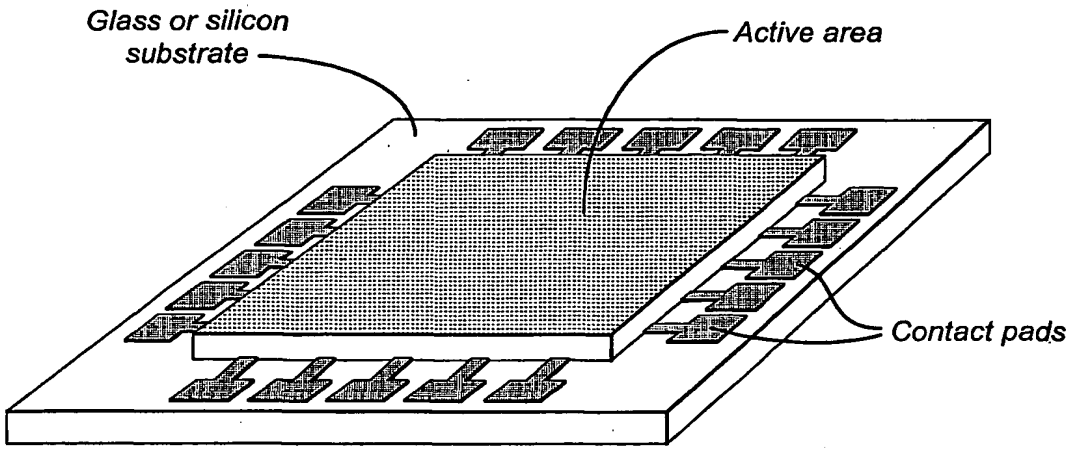

Fig. 1 Prior Art

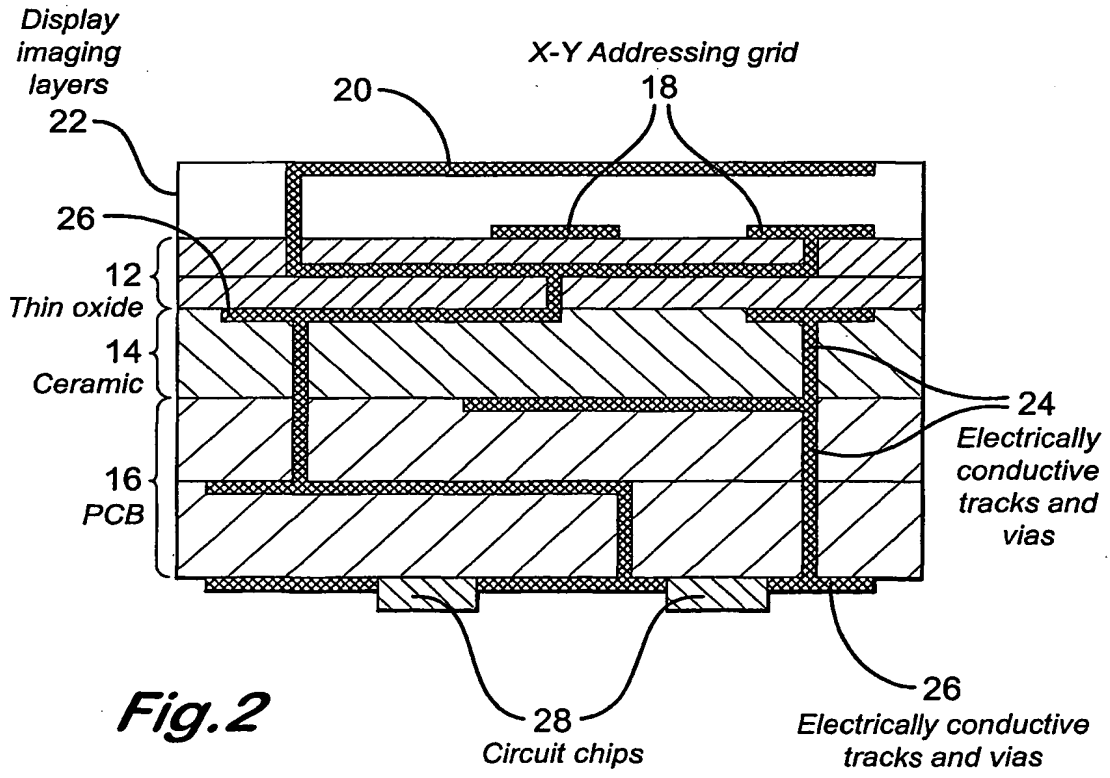

Fig. 2

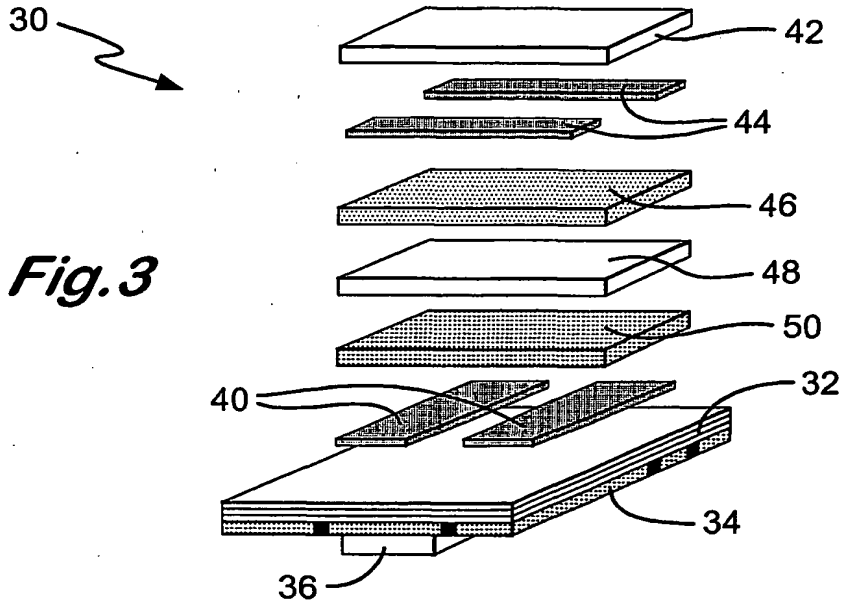

Fig.3

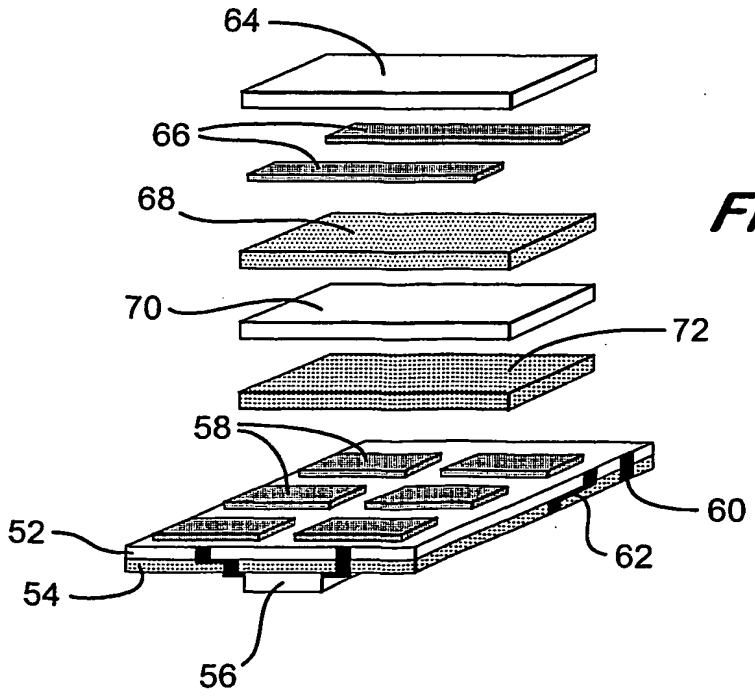

Fig.4

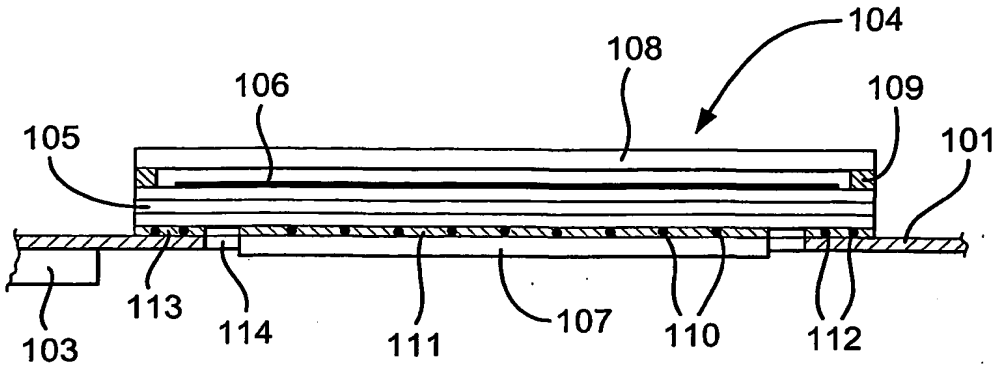
104
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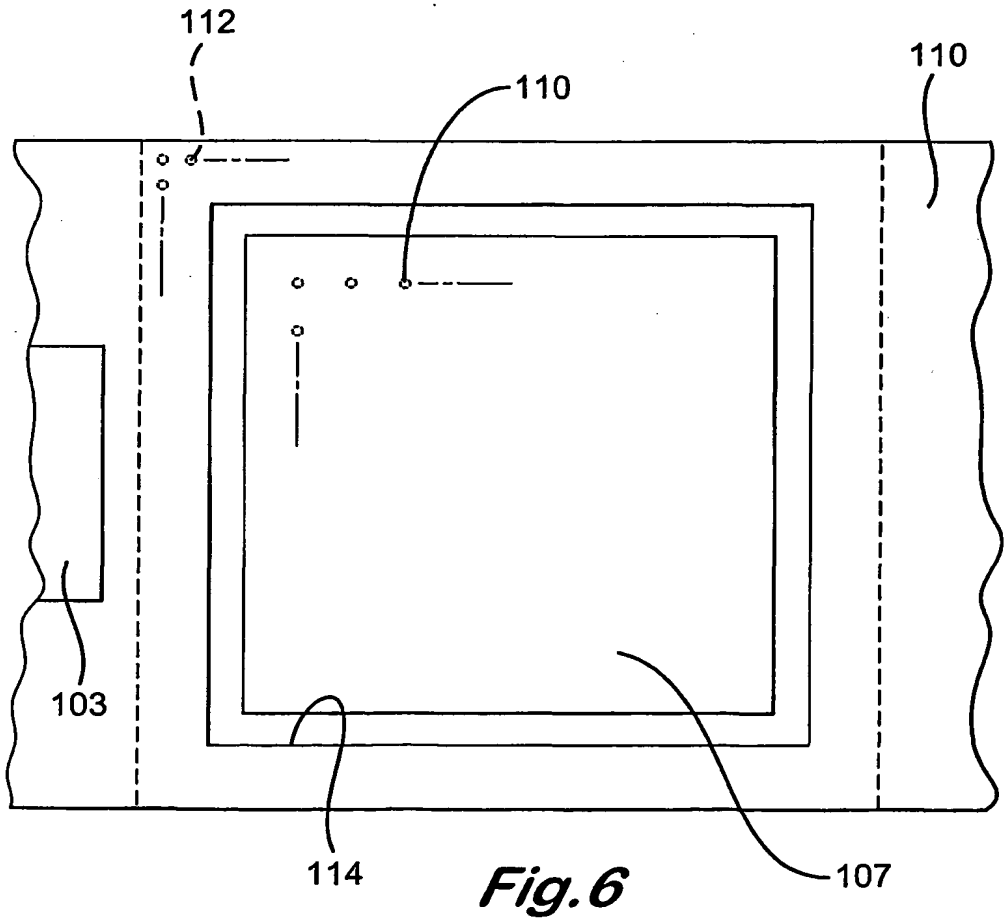
Fig.5


112
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103
114
107

Fig.6

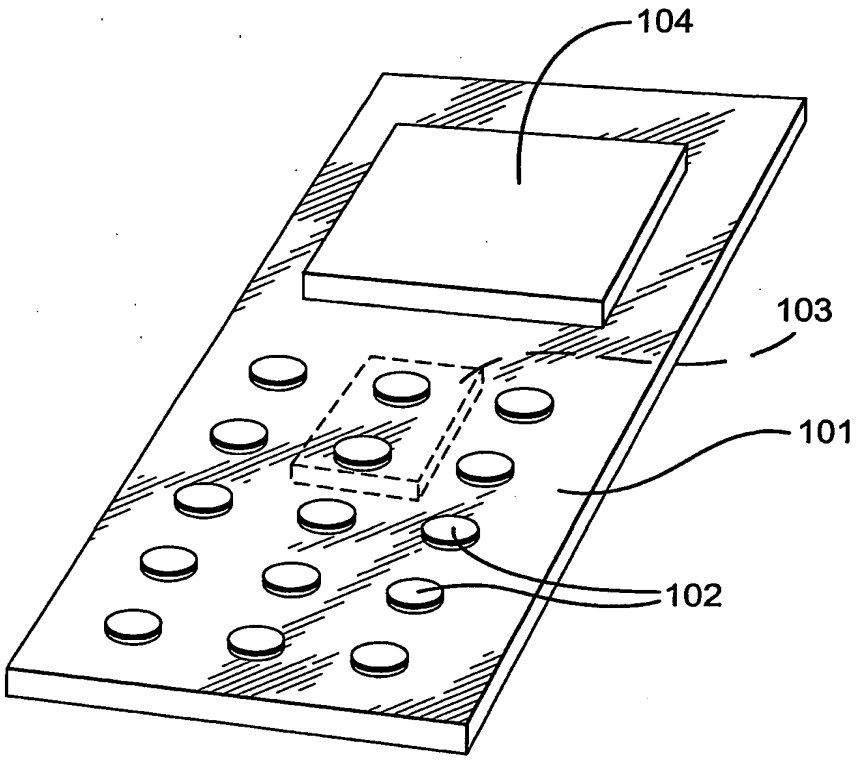

Fig. 7

INTERNATIONAL SEARCH REPORT

National Application No
PCT/US 00/24936

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01J29/92 H01J31/12 H01J5/52 H01L27/148

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01J H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 672 083 A (LOVOI PAUL A ET AL) 30 September 1997 (1997-09-30) column 4, line 57 - line 65 column 7, line 51 - line 64 column 9, line 59 -column 12, line 63 column 19, line 66 -column 20, line 22	1-8,18
Y		9,10,12, 14
X	WO 99 17330 A (SCREEN DEVELOPMENTS LTD ;COOPER ANTHONY JOHN (US)) 8 April 1999 (1999-04-08) cited in the application page 3, line 5 -page 4, line 29 page 12, line 2 -page 13, line 21; figure 1	1-6,8,18
Y		9,10,12, 14

☐ Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
6 June 2001	13/06/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	F de Ruyter-Noordman

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